gratings present certain problems, they can be useful in dielectric waveguide devices such as filters.

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Temperature Stabilization of GaAs MESFET Oscillators Using Dielectric Resonators

CHRISTOS TSIRONIS, MEMBER, IEEE, AND VLAD PAUKER

***Abstract*—A simple model of the temperature stabilization of dielectric resonator FET oscillators (DRO's) is presented. Deduced from the oscillation condition, the model furnishes relations for oscillation power and frequency stability with temperature.**

A stack resonator with an appropriate linear resonance frequency/temperature characteristic has been developed and used to stabilize a DRO: frequency stability of ±120 kHz over −20°C to 80°C (≙ ±0.1 ppm/K) at 11.5 GHz has been achieved.

I. INTRODUCTION

The availability of highly stable low-loss dielectric material has led to the development of a family of microwave solid-state signal sources: the dielectric resonator oscillators (DRO's).

The frequency stability with temperature of a GaAs FET DRO with the dielectric resonator coupled as a band rejection filter at the output port has been analyzed in [1] and for a Gunn-diode DRO in [2]. However, the highest stability with temperature has been reported in [3] for a reflection type FET DRO.

It is the aim of this paper to present an approach to temperature stability modeling of DRO's different from those described in [1], [2] and resulting in a model that furnishes concepts and limits for frequency stabilization, oscillation power, and requirements for an optimum resonator material. As an example, a very stable DRO with a GaAs FET chip from RTC (CFX 21 X) will be presented.

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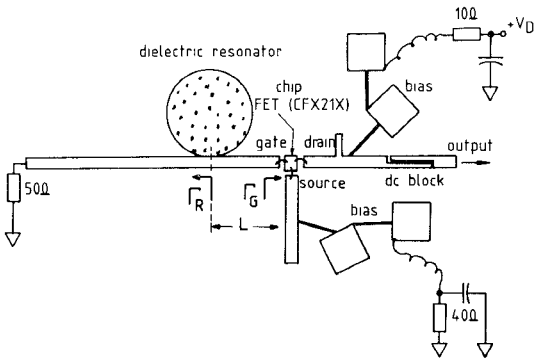

Fig. 1 Layout of FET dielectric resonator stabilized oscillator.

II. STABILIZATION MODEL

The reflection type FET DRO treated in our analysis is shown in Fig. 1. It is a common source configuration with capacitive series feedback that presents at the gate port a negative impedance

$$Z_G = -R_G + \frac{1}{j\omega C_G}$$

corresponding to the reflection coefficient

$$\Gamma_G = |\Gamma_G| \cdot e^{j\varphi_G} \quad \text{with } |\Gamma_G| > 1.$$

From this point of view, the analysis is valid for any DRO circuit that can be described this way. The impedance of a matched microstrip line coupled with a dielectric resonator (Fig. 1) can be calculated at the plane of the resonator as

$$Z_R = Z_0 + Z_0 \cdot \beta \Big/ \left(1 + 2j \cdot \frac{f - f_r}{f_r} Q_r\right). \tag{1}$$

The corresponding reflection coefficient is

$$\Gamma_R = \beta \Big/ \left(2 + \beta + 4j \cdot \frac{f - f_r}{f_r} \cdot Q_r\right) \tag{2}$$

with β the coupling factor between dielectric resonator and microstrip line, f_r and Q_r the resonance frequency and unloaded Q-factor of the dielectric resonator when coupled to the microstrip line, and Z_0 the characteristic impedance of the line. At the plane of the FET, Γ_R appears transformed by the microstrip line L to

$$\Gamma_R' = \Gamma_R \cdot e^{-j\tau f} \quad \text{with } \tau \approx 1.07 \cdot L \cdot 10^{-10} \text{s/mm}. \tag{3}$$

The oscillation condition is now applied at the plane of the gate port

$$\Gamma_R' \cdot \Gamma_G = 1 \tag{4}$$

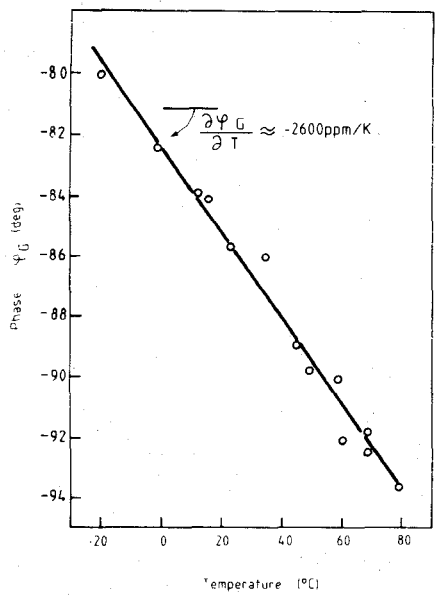

Fig. 2. Device phase drift with temperature measured into the gate port for constant modul $|\Gamma_G|$ of the reflection coefficient. φ_G is expressed in radians.

or

$$\frac{\beta}{2+\beta+4j\dfrac{f-f_r}{f_r}Q_r}\cdot e^{-j\tau f}\cdot|\Gamma_G|\cdot e^{j\varphi_G}=1. \tag{5}$$

Splitting this equation into real and imaginary parts, we obtain

$$\beta\cdot|\Gamma_G|\cdot\cos(\varphi_G-\tau f)=2+\beta \tag{6}$$

and

$$\beta\cdot|\Gamma_G|\cdot\sin(\varphi_G-\tau f)=4\cdot\frac{f-f_r}{f_r}\cdot Q_r. \tag{7}$$

Introducing (6) into (7), the oscillation frequency condition results

$$\frac{2+\beta}{4Q_r}\cdot tg(\varphi_G-\tau f)=\frac{f-f_r}{f_r}. \tag{8}$$

The temperature stability of the oscillation frequency can be obtained from (8)

$$\frac{\partial[(\beta+2)/4Q_r)]}{\partial T}\cdot tg(\varphi_G-\tau f)+\frac{\beta+2}{4Q_r}\cdot\left(\frac{\partial\varphi_G}{\partial T}-\tau\frac{df}{dT}\right)\cdot\left[1+tg^2(\varphi_G-\tau f)\right]=\frac{df}{f_r dT}-\frac{df_r}{f_r^2 dT}\cdot f. \tag{9}$$

For optimum positioning of the dielectric resonator ($f\approx f_r$), the terms

$$4\cdot\frac{f-f_r}{f_r}\cdot\frac{Q_r}{\beta+2}$$

being the equivalent of $tg(\varphi_G-\tau f)$ in (8), is much less than unity. It has been found experimentally that

$$\frac{\partial}{\partial T}\left(\frac{\beta+2}{4Q_r}\right)$$

is 5 to 10 times smaller than $\partial\varphi_G/\partial T$, and $\tau\cdot(df/dT)$ is negligible in comparison to $\partial\varphi_G/\partial T$. The simplified form of the temperature stability of DRO's becomes therefore

$$\frac{df}{f\,dT}\approx\frac{df_r}{f_r dT}+\frac{\beta+2}{4Q_r}\cdot\left.\frac{\partial\varphi_G}{\partial T}\right|_{|\Gamma_G|=\text{const}}. \tag{10}$$

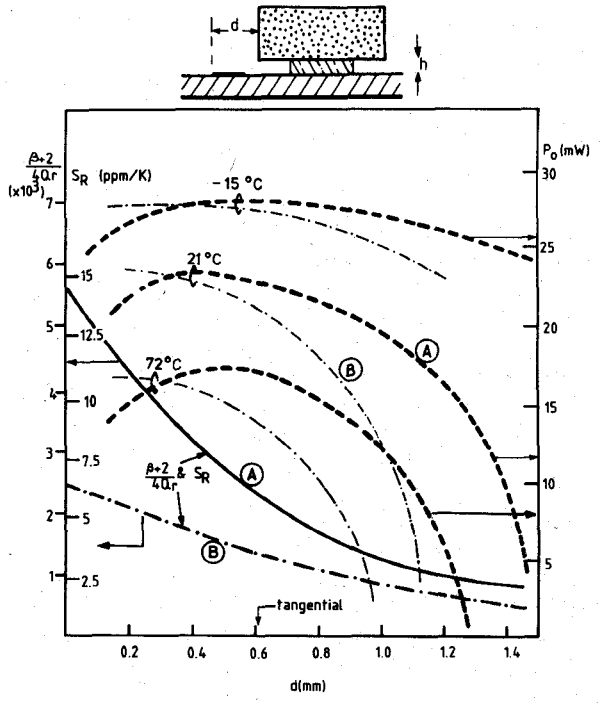

Fig. 3. Coupling-Stability-Power-Temperature diagram for FET DRO's. Values are given for the stacked resonator with low Q_r ($\approx$ 1000–2000 in case *B* and 600 to 1500 in case *A*). The device drift is assumed to be −2600 ppm/K.

Fig. 2 shows

$$\left.\frac{\partial\varphi_G}{\partial T}\right|_{|\Gamma_G|=\text{const}}$$

to have values of −2000 to −3000 ppm/K, while in Fig. 3, $(\beta+2)/4Q_r$ is shown to vary between 10^{-3} and 6.10^{-3}, depending on the coupling between the dielectric resonator and the microstrip line and on the mounting method of the dielectric resonator on the substrate.

Using the above approximations, we obtain from (6) the oscillation power condition

$$|\Gamma_G|=|\Gamma_G(P,T)|\approx\frac{\beta+2}{\beta}\approx\text{const}|_T. \tag{11}$$

Since $|\Gamma_G(T)|$ and $|\Gamma_G(P)|$ are monotonically decreasing functions, (11) suggests that at higher temperatures the device will decrease its oscillation power in order to keep satisfied the condition (11). This is also illustrated in Fig. 3.

III. Results

The diagram of Fig. 3, containing only measured quantities, shows the stabilization procedure. The resonator stability

$$S_R=\frac{df_r}{f_r dT}$$

needed for a completely stable oscillator

$$\left(S_0=\frac{df}{f\,dT}=0\right)$$

as well as the stabilization factor $(\beta+2)/4\ Q_r$ are given on the left axis as a function of coupling (d) between the dielectric resonator and the microstrip line for two different mounting conditions: 1) the resonator is posed directly on the Al_2O_3 substrate; and 2) the resonator is posed on a 0.5-mm-thick quartz spacer. The proportionality factor between these two quantities is

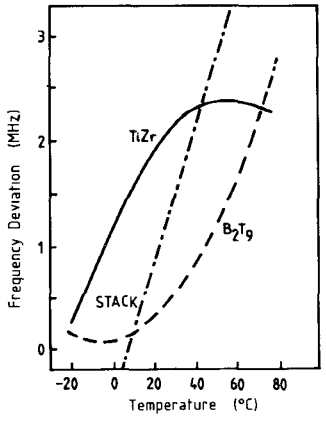

Fig. 4. Temperature characteristic of different dielectric resonator materials.

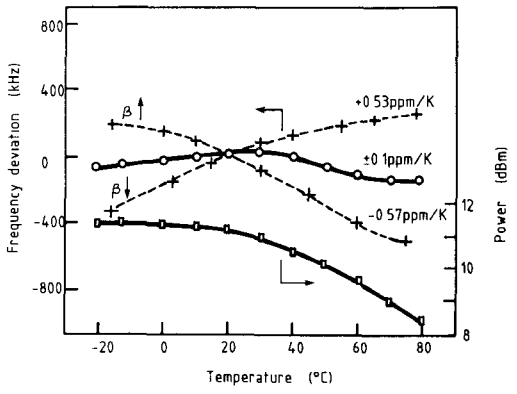

Fig. 5. Performance of ultra-stable FET DRO and influence of coupling factor β on temperature stability. Frequency: 11.518 GHz.

the device drift $\partial\varphi_G/\partial T$ as follows from (10). On the right axis of the diagram, the oscillation power[1] is given, measured for three different temperatures (21°C and for the extreme cases of −15°C and 72°C): besides the stability S_R of the resonator necessary for overall compensation as a function of coupling (d), the diagram also gives the expected power variation with temperature under the same conditions.

A. Example

For $d = 0.8$ mm, we obtain in case A an S_R of 4.4 ppm/K and in case B, 2.9 ppm/K. This is due to the higher Q_r of the resonator mounted on the quartz spacer. The maximum power variation with temperature will be 27 mW to 15 mW in case A (2.6 dB) and 26 mW to 10 mW in case B (4.2 dB). This example shows also the limits for stabilization given by the variation of the oscillation power with temperature: for a weaker coupling ($d = 1.2$ mm, for instance), a dielectric resonator with an S_R of 2.8 ppm/K would be sufficient from compensation point of view, the power variation, however, will be too large and the oscillation won't be sustained at 70°C. For the same performance concerning the power variation, a decrease of material slope S_R has to be compensated by an increase of quality factor Q_r according to

$$\frac{\beta+2}{4Q_r} = \left|\frac{S_R}{\partial\varphi_G/\partial T}\right| \tag{12}$$

where β (or d in Fig. 3) has to be kept constant.

Because of the constant temperature drift ($\partial\varphi_G/\partial T$) of the phase of the reflexion coefficient at the gate port, it can be concluded from (10) that S_R of the resonator has to be constant over the regarded temperature range, here −20°C to 80°C. Tested Barium–nona–Titanate and Titanium–Zirconate resonators showed a minimum at 0°C and a maximum at 40°C, respectively, of their $f_r(T)$ characteristics (Fig. 4). That means that the corresponding $S_R(T)$ varies strongly and is not appropriate for compensation in that temperature range. The $f_r(T)$ curves being nearly inverse, we developed a stack resonator composed of two cylinders of these two materials 5 mm in diameter and 1 mm high, having linear $f_r(T)$ characteristic from −20°C to 80°C with a slope $S_R \approx 6$ ppm/K, when characterized in the actual oscillator metallic mounting, that has a nonnegligible influence on quality factor Q_r and resonator drift S_R due to thermal dilatation.

Using this resonator, we stabilized a FET DRO of the type shown in Fig. 1. Varying the coupling between resonator and microstrip line results in an overall stability S_0 between 0.5 and −0.5 ppm/K (Fig. 5). For an intermediate position of the resonator, the best result given in Fig. 5 was achieved: ±0.1 ppm/K corresponding to an overall frequency variation of ±120 kHz over −20°C to 80°C.

IV. Conclusion

A simple approach to frequency stabilization of DRO's is presented. Model parameters preferably measured *in situ* are: the resonator drift S_R, its unloaded Q and coupling with the microstrip line β, and the active circuit phase temperature drift $\partial\varphi_G/\partial T$. Conditions for appropriate dielectric material and limits of stabilization also in view of oscillation power are given. Using a BaTi/TiZr composed resonator, a FET DRO with a CFX 21X FET chip (RTC) with ±0.1 ppm/K over −20°C to 80°C has been realized.

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[1] The oscillation power is estimated as

$$P_0 = P_D + P_G\left(|\Gamma_G|^2 - 1\right)$$

where P_D is the power leaving the drain port, and P_G the power injected into the gate port [4].